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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,811	GRAETTINGER ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *78-89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *78-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 78-89 are objected to because of the following informalities and/or defects:

In claim 78, the term of "thereby protecting the conductive connector" fails to clearly and definitely define what is the subject that protects the recited conductive connector.

In claims 84 and 87, the term of "barrier to corrosion" should read as: --barrier against corrosion--.

In claim 84, the term of "other surfaces of the contact hole" is not clearly defined in the disclosure.

In claim 88, the term of "surrounding" should read as: --covering--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 78, 80 and 82-83, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner et al. ("Hartner"; WO 98/15013; also see US 6,043,529 for its English translation; both are in record) in view of Juengling (US 5,700,706)

Hartner discloses a method for protecting conductive elements (such as plugs) from potential adverse oxidation during the annealing of a high dielectric constant layer (6) in a capacitor (see Fig. 2, col. 23, lines 63-67, and col. 1, line 30, through col. 2, line 17, in US 6,043,529), comprising the steps of: forming a gate (13); forming a silicon nitride barrier liner (16) covering the inner sidewalls of a contact opening in a dielectric interlayer (2); and forming conductive connector(s) or plug(s) (1) inside the silicon nitride barrier liner (16), wherein the conductive connect(s) or plug(s) electrically connect(s) the capacitor (5-6; an upper circuit element) to a transistor active region (9; a lower circuit element).

Although Hartner does not expressly disclose that the method can further comprise the step of forming an insulating barrier liner covering the gate and in contacts with the a silicon nitride barrier liner, one of ordinary skill in the art would readily recognize that the gate can be preferably covered by an insulating barrier liner for better protection to the gate and for better alignment among the gate, channel and source/drain regions, and that the liner for the gate and the liner for the plug can be in contact for reducing size, as both evidenced in Juengling (see the silicon nitride gate liner 24 and silicon nitride plug liner 54 in Figs. 2 and 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make a semiconductor device of Hartner with the method further comprising the step of forming a silicon nitride gate liner (the insulating barrier liner) in contact with the silicon nitride (plug) barrier liner, as taught in Juengling, so that a method for making a semiconductor device with better protection to the gate and better structure alignment and with reduced size would be achieved.

Regarding claim 82, the capacitor dielectric layer in Hartner can be formed with a ferroelectric material (see col. 1, lines 61-67), which would naturally have a dielectric constant greater than about 10.

4. Claim 79, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner in view of Juengling, as applied to claims 78, 80 and 82-83 above, and further in view of Cho et al. ("Cho"; US 5,346,844; of record).

The disclosure of Hartner and Juengling are discussed as applied to claims 78, 80 and 82-83 above.

Although Hartner and Juengling do not expressly disclose that portions of the gate can be in contact with the silicon nitride (plug) barrier liner, one of ordinary skill in the art would readily recognize that such a silicon nitride (plug) barrier liner can be in contact with portions of the gate for further reducing the device size, as evidenced in the prior art such as Cho (see the gate electrode (18) in direct contact with the silicon nitride plug liner (40) in Fig. 3A)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above collectively taught method to make a semiconductor device with portions of the gate being in contact with the silicon nitride (plug) barrier liner, as taught in Cho, so that a method for making a semiconductor device with better protection to the gate and better structure alignment and with reduced size would be achieved.

5. Claim 81, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner in view of Juengling, as applied to claims 78, 80 and 82-83 above, and further in view of Sun et al. ("Sun"; US 4,926,237).

The disclosure of Hartner and Juengling are discussed as applied to claims 78, 80 and 82-83 above.

Hartner further teaches to form a conductive barrier liner (3) on top of the electrical connector (plug).

Although Hartner and Juengling do not expressly disclose that the method can further comprise the step of forming a conductive barrier liner between the silicon nitride barrier liner and the electrical connector (plug), Sun teaches that an electrical plug (28) formed inside a dielectric layer (16, including silicon nitride, see col. 3, lines 12-14) can desirably have a conductive diffusion barrier liner (22, 26, and/or 24) disposed therebetween, i.e., forming the conductive diffusion barrier prior to the formation of the

plug, which also naturally forms a conductive barrier liner at the bottom of the electrical plug, for providing better protection to the electrical plug.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the step of forming the conductive barrier liner of Sun into the above collectively taught method, so that a method for making a semiconductor device with better protection to the electrical plug would be obtained.

6. Claims 84-87, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner et al. ("Hartner"; WO 98/15013; also see US 6,043,529 for its English translation; both are in record) in view of Sun et al. ("Sun"; US 4,926,237).

Hartner discloses a method for protecting conductive elements (such as plugs) from potential adverse oxidation during the annealing of a high dielectric constant layer (6) in a capacitor (see Fig. 2, col. 23, lines 63-67, and col. 1, line 30, through col. 2, line 17, in US 6,043,529), comprising the steps of: forming a gate (13); forming a second barrier (16, silicon nitride barrier liner) covering the inner sidewalls of a contact opening in a dielectric interlayer (2); and forming a conductive contact plug (1) inside the silicon nitride barrier liner (16); and forming a capping barrier(3; readable as the third barrier recited in claim 73), wherein the conductive contact plug electrically connects the capacitor (5-6; an upper circuit element) to a transistor active region (9; a lower circuit element).

Although Hartner does not expressly disclose that the method can further comprise the step of forming a first barrier (a conductive barrier liner) between the second barrier (the silicon nitride barrier liner) and the contact plug, Sun teaches that a contact plug (28) formed inside a dielectric layer (16, including silicon nitride, see col. 3, lines 12-14) can desirably have a first barrier (a conductive diffusion barrier liner, 22, 26, and/or 24) disposed therebetween, i.e., forming the conductive diffusion barrier prior to the formation of the plug, which also naturally forms a conductive barrier liner at the bottom of the electrical plug, for providing better protection to the electrical plug.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporating the step of forming the conductive barrier liner of Sun into the method of Hartner, so that a method for making a semiconductor device with better protection to the contact plug would be obtained. And, with the first barrier (the conductive diffusion barrier) being formed prior to the formation of the plug in the above collectively taught device, the first barrier would be naturally formed between the second barrier and the plug; and the bottom barrier would be naturally formed between the plug and the transistor active area in the substrate.

Regarding claim 88, it is noted that one of ordinary skill in the art would readily recognize that the gate (i.e., a bit or word line) can be preferably covered by an insulating layer including a sidewall portion and a cap portion for better protection to the gate and for better alignment among the gate, channel and source/drain regions, as evidenced in the prior art such as Juengling (see the silicon nitride gate liner 24 in Figs. 2 and 6).

7. Claim 89, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartner in view of Sun, as applied to claims 84-88 above, and further in view of Cho et al. ("Cho"; US 5,346,844; of record).

The disclosure of Hartner and Sun are discussed as applied to claims 84-88 above.

Although Hartner and Sun do not expressly disclose that portions of the gate (i.e., a bit or word line) can be in contact with the silicon nitride (plug) barrier liner (i.e., the second barrier), one of ordinary skill in the art would readily recognize that such a silicon nitride (plug) barrier liner can be in contact with portions of the gate for further reducing the device size, as evidenced in the prior art such as Cho (see the gate electrode (18) in direct contact with the silicon nitride plug liner (40) in Fig. 3A, wherein the method for making the device in Cho further including the step of forming an insulating layer (20) including a sidewall portion and a cap portion covering the gate electrode (18))

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the above collectively taught method to make a semiconductor device with portions of the gate being in contact with the silicon nitride (plug) barrier liner being in contact with silicon nitride (plug) barrier liner, as taught in Cho, so that a method form making a semiconductor device with reduced size would be achieved.

Response to Arguments

8. Applicant's arguments filed on 9/13/03 have been fully considered but they are not persuasive. As explained below.

Applicant's main arguments include that US Patent 6,043,529 to Hartner is not a valid prior art reference. In response, it is noted that the obviousness rejections set forth in the previous Office action, and in this one as well, are based on Hartner et al. ("Hartner"; WO 98/15013, which is published on April 9, 1998) in combination with various other references. The US Patent 6,043,529 to Hartner is provided only for the convenience to the applicant, as it provides an English translation for WO 98/15013.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
November 18, 2003

SHOUXIANG HU
PRIMARY EXAMINER